INTERSIL

Bipolar PROM Programming Specification

PROGRAMMING PROCEDURES

1. Prior to beginning a programming cycle, the part to be grammed must be searched for previously programmed bits. This must be done to eliminate the risk of programming a part that has some bits not conforming to the pattern desired.
2. Programming is begun by addressing the first word in the sequence, normally address ZERO, although satisfactory programming is not dependent on the word sequence or bit order used.
3. Disable the device by applying a normal TTL high logic level to any active low CE pin. Disabling the device forces the normal output circuitry to a high impedance condition so that it will not be affected by programming pulses applied through the output pins to the programming element array.
4. Sense the bit status by forcing 20mA into the associated output pin and comparing the resultant voltage to the SENSE VOLTAGE.
5. If the bit is to be programmed, increase the 20mA to 200mA at the proper ramp rate and maintain 200mA for 7.5μs. The constant current source must be clamped at 28V.
6. Reduce the current from 200 to 20mA and after 1μs compare the resultant 20mA voltage level to the SENSE VOLTAGE.
7. If the voltage is greater than the SENSE VOLTAGE the current should be increased again to 200mA for another 7.5μs. Generally, programming occurs on the first pulse, but repeated attempts are allowed up to an elapsed time of 100ms.

PROGRAMMING PARAMETER SPECIFICATIONS

The following specification details the necessary requirements for the correct programming of the IM56XX Series of AIM PROMs. Intersil will not accept responsibility for any device found to be defective if it was not programmed according to these specifications.

PARAMETER	LIMITS MIN	NOM	MAX	UNITS	CONDITIONS
Programming Current Pulse Amplitude	190	200	210	mA	Constant current to be supplied over a 10 to 28V voltage range. Set the nominal value with a 100Ω, 6W load @ 20V.
Voltage Clamp	27.5	28	28.5	Volts	Constant voltage clamp when sinking 130 to 210 mA. Adjust nominal level when sinking 200 mA.
Ramp Rate $\frac{dv}{dt}$ of Program Current Source	50	60	70	V/μs	Voltage ramp rate is measured by switching from 20 to 200 mA into a 100 ohm, 6W resistor with the maximum voltage clamped at 28V.
Pulse Width	7.0	7.5	8.0	μs	Measured at 10V when switching between 20 and 200 mA into a 100 ohm, 6W load resistor.
Duty Cycle	70	75	80	%	Measured at 10V when switching between 20 and 200 mA into a 100 ohm, 6W load resistor.
Sense Current Amplitude	19.5	20.0	20.5	mA	Constant current source amplitude is adjusted for a nominal value of 20 mA into a 12V, 400 mW zener diode load.
Ramp Rate $\frac{dv}{dt}$ Sense Current Source	50	60	70	V/μs	Voltage ramp rate is measured by switching from 0 to 20 mA into a 1.5k ohm, 1W resistor with the maximum voltage clamped at 28V.
Sense Voltage Analog Comparator Reference Voltage	6.9	7.0	7.1	Volts	An element is considered programmed when the voltage sensed at the appropriate output pin with 20 mA forced through the element is less than the analog comparator reference voltage.
5600/10 Only	12.4	12.5	12.6	Volts	
Min. delay from trailing edge of programming pulse before sensing	0.9	1.0	1.1	μs	Measured from the 10V level of the voltage pulse when switching from 200 to 20 mA into a 100 ohm, 6W load resistor.
Vcc	4.9	5.0	5.5	Volts	100 to 200 mA current range.
Programming Time Allocation/Bit	—	100	—	ms	Maximum time allowed to program a bit.
Extra Programming Pulses	—	4	—	Pulse	Absolute number of programming pulses to be issued after the bit output is first sensed as a programmed '1'. This occurs when the sensed voltage is less than the comparator reference voltage.

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PROGRAMMING PROCEDURES (Continued)

8. If the voltage after a programming current pulse is less than the SENSE VOLTAGE, four additional programming pulses are applied with a sense after each pulse.
9. After the fourth extra pulse and correct sense, programming is complete. The 20mA current pulse then is shut off and the address is changed to program the next bit.
10. Repeat steps 4 thru 9 until a successful programming and sense operation is performed at all address locations to be programmed.
11. After the programming cycle is complete, a logical verification must be performed. This is done by cycling through all address locations with the chip enabled and testing the voltage level at each output under the appropriate current forcing condition (20mA for a low level and 100μA for a high level). This cycle should be completed at both low and high V_{CC}.

POST PROGRAMMING LOGICAL VERIFICATION

Both high (V_{OH}) and low (V_{OL}) logic levels on all outputs should be tested. For all truth-table addresses two passes must be made, one with V_{CC} high and one with V_{CC} low. Forcing conditions and limits for level testing are specified in the following tables.

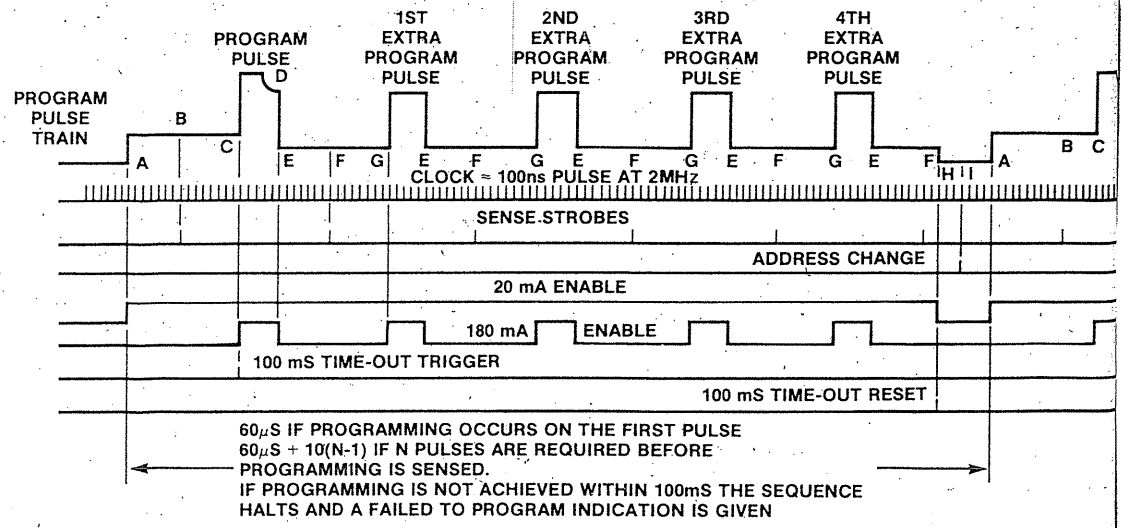
HIGH V_{CC} TESTS — V_{CC} = 6.5 ± .1V

PARAMETER	LIMIT MIN	LIMIT MAX	FORCING CONDITION	LEVEL TESTED
V_{OL}	—	.85	I_{OL} = 20mA ± 1mA	Zero
V_{OH}	6.9	—	I_{OL} = 100μA ± 10μA	One

LOW V_{CC} TESTS — V_{CC} = 4.0V ± .1V

PARAMETER	LIMIT MIN	LIMIT MAX	FORCING CONDITION	LEVEL TESTED
V_{OL}	—	.85	I_{OL} = 20mA ± 1mA	Zero
V_{OH}	4.5	—	I_{OL} = 100μA ± 10μA	One

PROGRAMMING CYCLE TIMING DIAGRAM



A - 20mA CURRENT SOURCE TURNED ON (VOLTAGE OVERSHOOT MAY OCCUR)
B - VOLTAGE LEVEL IS SENSED AND COMPARED
C - 180mA CURRENT SOURCE IS TURNED ON (180 + 20 = 200mA)
D - VOLTAGE FALLS INDICATING PROGRAMMING
E - 180mA CURRENT SOURCE IS TURNED OFF
F - VOLTAGE LEVEL IS SENSED AND COMPARED
G - 180mA CURRENT SOURCED IS TURNED ON
H - 20mA CURRENT SOURCE IS TURNED OFF
I - ADDRESS IS CHANGED

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